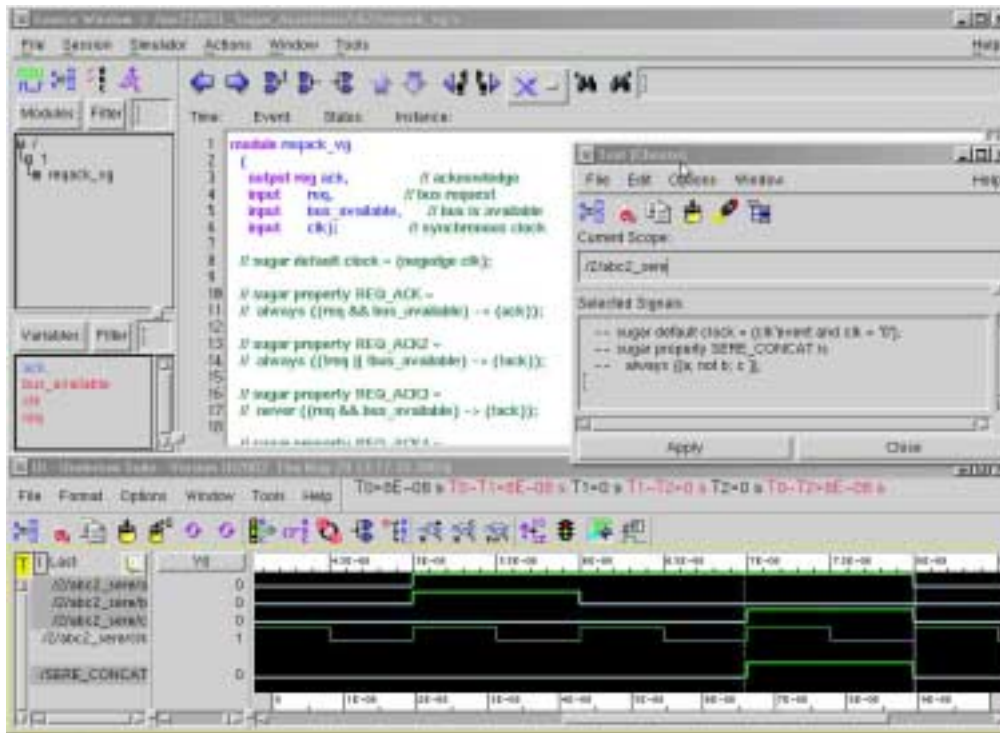


Undertow Suite with Sugar/Open Vera

Veritools' design solutions now includes integration with Open Vera and Sugar assertion languages.

PSL/



Undertow Suite with Sugar/Open Vera integration includes these important features:

This integration includes the Open Vera Assertions, and the Property Specification(PSL) language Sugar, for assertion based verification of Verilog or VHDL designs. For PSL, this integration includes verifying design properties, using the Boolean layer, the temporal layer, the verification layer, and even the modeling layer of this language. Currently the modeling layer is only defined for the Verilog language. Veritools integrates these languages in a unique way, the Open Vera/PSL/Sugar is translated to the internal language for the Undertow Suite, PERL/TK, for use with the very high speed Perl scripting capability that is built directly into the Undertow Suite.

Once the translation is completed, in most cases a process that takes just seconds, this resultant Perl code can be run in either an interactive mode, while the GUI is open or in a pure batch process as part of automatic scripts, with no GUI up at all and no intervention from a user while running. The output results from the running of the OVA/PSL/Sugar can be either a resultant table of the OVA/PSL/SUGAR results and/or annotated waveforms that can be viewed using the Undertow waveform window portion of the Undertow Suite software. If the OVA/PSL/Sugar assertions are run in a batch process, and they indicated some conditions were in error or not correct states, the result file can be

read back into the Undertow Suite to re-annotate the waveform display in order to show the exact point in the waveform file of the error conditions.

Since the OVA/PSL/Sugar code is run on the simulation resultant files, after the simulation is done, and not run during simulation, which would add significant simulation overhead, they do not have any impact at all on simulation run times or speed. The OVA/PSL/Sugar assertions can be run as many times as is necessary on the simulation result files without tying up a simulation license, or requiring any additional simulation runs unless the original design or test vectors have been changed. This allows users to do assertion based analysis with little on no additional impact on the simulation run times or simulation runs, in fact since different OVA/PSL/Sugar assertions can be run on the same simulation output file, the required number simulation runs in order to fully verify any design could be significantly reduced. Virtually no other approach will provide this level of verification with a simultaneous significant reduction of simulation operations, with the potential for providing a significant reduction in a companies CAD costs, while at the same time significantly adding to the completeness of the verification.

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Download Undertow Suite from our web site: www.veritools.com

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