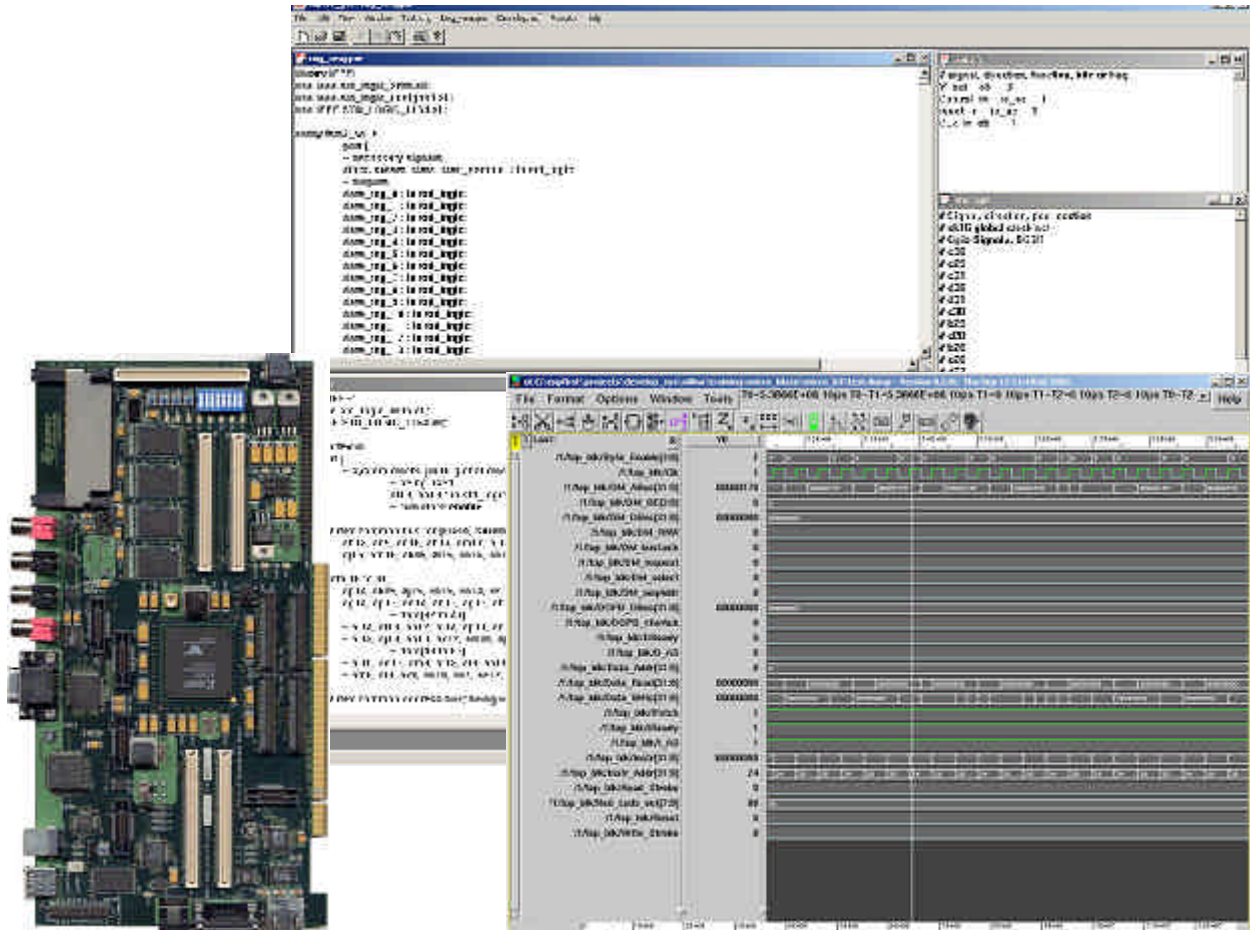


FPGA Logic_Analyzer

** Logic Analyzer for FPGAs* Automatic Test Bench Generation for FPGAs* Real Time Signal Data Collection for FPGAs * Designer uses same tool for the design and debug of their*



The Undertow FPGA Logic Analyzer 9.2 includes these following features:

Kit Includes:

- * Includes Xilinx Virtex- E Development Platform and software
- * Includes a cable for PC/PCI and development system PCB for the Xilinx Virtex FPGA
- * Includes a complete and powerful waveform viewer with source code debugging capability with RTL schematics

Features:

- * Supports Xilinx Virtex FPGA development

- * Over 445 user I/Os for System Testing
- * Both VCD/Fast File Generation Capability
- * USB Interface for high speed data transfer
- * Complete waveform and interface Software
- * Complete Hardware System with PCI Bus, USB, Memory, JTAG, RS-232, and Video
- * Uses a USB2 bus, very compressed “fast files” and a very powerful waveform viewer, to provide the absolute fastest possible debugging platform

Download at www.veritools-web.com

Veritools 459 Hamilton Ave., Suite 200, Palo Alto, CA 94301

phone: (650) 462-5590 fax: (650) 462-5593 email: inquiry@veritools.com download: www.veritools-web.com

The Undertow FPGA Logic Analyzer system provides one of the most powerful systems on the market today to allow a designer **to process, load and debug their FPGA design**. This greatly enhances your engineering teams productivity and can greatly accelerate your time to market.

The Undertow FPGA Logic Analyzer Development Environment is an integrated software, firmware and the complete hardware PCB to allow a designer to process, download the design onto the development PCB and then test their Virtex FPGA design. This development system allows the designer to accelerate the development, integration, and testing their own designs or commercial IP based Xilinx FPGA designs.

Automatic Logic Insertion - This suite of tools automatically inserts logic around any IP core to route inputs and outputs to real-time input signals, output signals, and buffer memory available on the development board. This allows the core to be exercised at 'hardware speeds'. Core output signals that are stored in the buffer memory can be read out over the USB port to the users host computer and displayed on the Undertow waveform viewer, just as if the core output signals were software simulation results. This approach to verification can significantly reduce the design/debug cycle time dramatically.

Immediate results from design and test changes - The Undertow FPGA Logic Analyzer Development Kit makes it easy to perform design or test set-up changes and see the results immediately. With the extensive hardware functions available on the kit, you can begin your FPGA design or applications code development right away, with no need to wait for prototype circuit boards. Also, while the user's IP is provided with real time stimulus from external system level hardware, The Undertow FPGA Logic Analyzer Development captures the response, and utilizes the live data to automatically create a test bench.

Much Faster Verification - Used in conjunction with a hardware-based input stimulus, verification of very complex and robust test suites are orders of magnitude faster than pure software simulation-based approaches. If observation and stimulus (on-chip, or at the system level) is required, a development system like the Undertow FPGA Logic Analyzer offers a hardware-based solution that you need to complete complex FPGA designs on schedule.

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