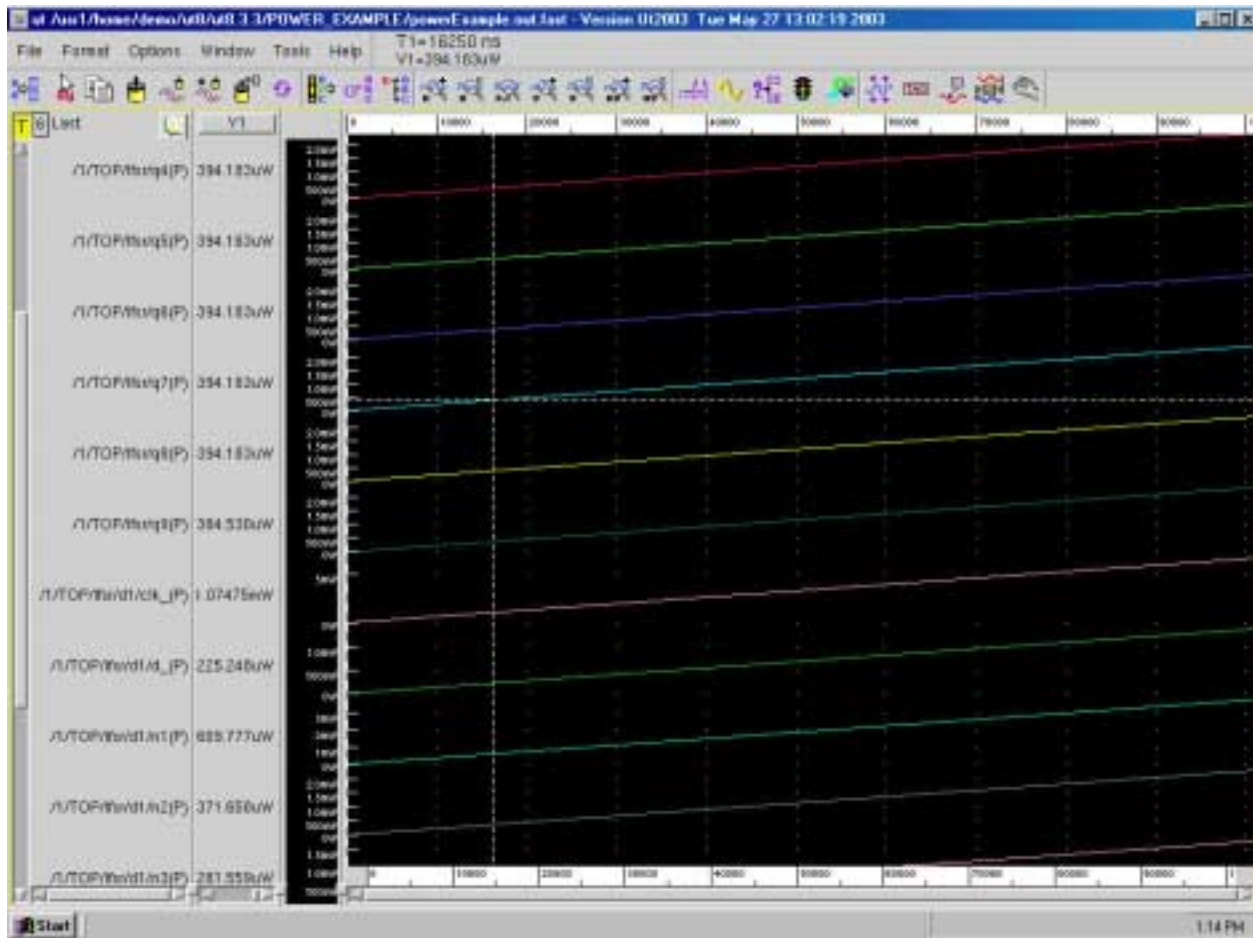


# RTL Power Analyzer

Veritools' Power Analyzer is targeted at providing power analysis for Verilog RTL designs.



Power Analyzer includes these important features:

- Power analyzer uses the gate and drain capacitance plus wire capacitance in order to very accurately calculate power
- Calculates power using standard simulation output results without slowing down the simulation in any way.
- Generates power calculation results on each node, element, block and module or sum of modules
- Generates power calculation results at 6 nanosecond intervals, these can be averaged over any two time points
- Power results can be in text or displayed on the very widely used waveform viewer, Undertow/Undertow Suite
- Allows the user to sort elements, and blocks by power consumed
- Includes a "Design Power Analyzer", so users can re-calculate power results instantly, after making a number of design changes



Download Power Analyzer from our web site: [www.veritools.com](http://www.veritools.com)

# Tools for Power Users

## Power Analyzer - General Information

The RTL Power analysis tool incorporates the powerful Veritool's HDLAnalyzer, a complete RTL synthesis tool that is currently used to create schematics from RTL source code for providing faster source code debugging with Undertow Suite. Since the synthesis is from RTL source code to RTL gates, the synthesis operation typically takes just a few seconds even on very large designs. Since this analysis is based on an actual synthesis of the users RTL source code to RTL gates, this tool provides a level of accuracy, with a power analysis speed that can be achieved with no other tool on the market.

## Power Consumption

Since every node in the design is checked for power consumption, there is no configuration required for setting up the tool.

Because power is calculated for every node, the power consumptions values can be summed up for any block, any module, or any combination of modules. Users can also investigate the power consumed in any block to find the power consumed by any element, FF, latch, or combinational logic. Users can get the designs total power, in "real" power numbers, view the power over any time interval at any point, or get the average between any two time points, and can then see exactly what element in any block are consuming exactly what amount of power, over what period of time. Designers do not have to be told what logic elements or groups of elements are consuming the most power, the power calculation numbers will show them instantly where the power is being consumed. They also sort by the amount of power consumed by any element, or block or module.

## Power Calculation

Power calculation information can be displayed as waveforms in milliwatts for each node, and can be averaged over any two time points and as average power consumption numbers annotated directly onto the RTL schematics, for any point in the simulation. Since there is always a one to one correlation between the RTL schematics and the RTL source code, designer can find instantly, the exact line of source code that is causing the high power conditions, and can then modify the logic to get lower power numbers. The user can then reanalyze, using the same exact simulation results in order to see what the Power reduction has been. No guessing is required in order to see what the exact power reduction is from any design alterations.

## Power Design Analyzer

Veritools also offers users a "Power Design Analyzer", an instant power re-calculator, that allows them to change logic in their design and get an instant analysis of exactly what the power reduction design change did to the resultant power consumption numbers. The design changes that can be checked with the Power Design Analyzer are reduction in clock frequency, gating of clocking circuits, plus the substitution of cells with different gate and/or drain capacitance.

When the design is finally synthesized, the users can then rerun the power tool on the exact gate design in order to get the final actual numbers from the final synthesized circuit.

The Power Analysis tool can handle designs employing any number of power and voltage domains. While the tool has not been priced as of yet, pricing will be commensurate with the quite reasonable pricing model typically found on the other Veritools software products.

**No other tool combines the accuracy with the speed at any price.**

All of the features of Undertow Suite are available in both interactive mode, or in batch mode for use in virtual simulation, without using a simulator license. Veritools products are available on 32 and 64 bit Sun \_Solaris, HP700/800, IBM AIX, in addition to Windows 98/NT/2000/XP and Linux systems. Copyright 2003, All Rights Reserved, Veritools, Inc. Trademarks are owned by their respective corporations.